

SPICE MODELING OF A FET-SWITCHED INDUCTION ACCELERATOR CELL*

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Abstract

A PSpice model of an induction accelerator cell switched by field-effect transistors (FETs) has been developed to simulate the modulator's circuit performance and induction core flux behavior. A FET switched induction cell has been built that generate 4-kV, 1 μ s pulses at pulse rates exceeding 100 kHz. The circuit architecture provides for core reset between pulses and produces bursts of pulses that are variable in amplitude, pulse width and prf. The transistor switching array, energy storage capacitors, reset circuit, and cell core are all combined into a compact, low-impedance package.

This high-prf induction cell is being developed as the accelerating element for a proposed heavy-ion recirculator, which is an arrangement of many small induction cells in a 30-m diameter circle. The recirculator will accept 10-MeV ions from a linear ion accelerator, under development at the Lawrence Berkeley Laboratory, and continue their acceleration to 60-MeV by repeatedly passing the ion beam through the many 5-kV cells. As the ions gain speed, the cell prf must also keep pace by increasing from 70 kHz to 200 kHz.

Simple PSpice models have been used to predict B-H loop behavior in the magnetic core and to analyze circuit performance. Simulations of the induction cell will be presented and compared with experimental data.

Introduction

Heavy-Ion Fusion

Heavy-ion accelerators are considered to be an alternative driver for inertial fusion [1]. In a heavy-ion inertial driver, multiple ion beams are accelerated to the kinetic energies needed for fusion target ignition. Several types of heavy-ion accelerators have been proposed as drivers including rf accelerators, linear accelerators, and recirculators [2]. The recirculator is an induction accelerator that accelerates ions in a closed path until the desired energy is achieved. This concept has considerable cost savings over other technologies because most of the accelerating components are re-used many times during a single accelerating sequence.

A test of recirculator physics and technology concept is proposed by attaching a recirculator experiment on to the ILSE accelerator (Induction Linac Systems Experiment) at the Lawrence Berkeley Laboratory (LBL) [3]. The proposed recirculator consists of many 5-kV accelerating cells arranged in a 30-m diameter circle. Ten MeV ions enter the recirculator from ILSE and are accelerated to approximately 60 MeV by passing through each induction cell many times.

Solid State Modulators

High pulse repetition rate modulators are required to drive the induction cells in the recirculator for ILSE. The modulators must be capable of repetition rates ranging from 70 kHz to 200 kHz with pulse durations from 1 μ s to 400 ns and be able to reset the cell between pulses. Because of the pulse agility required for the recirculator, the modulator must have command on-off capability so we are developing a modulator technology based on solid state devices. As part of this development effort, we have evaluated different solid state switches, gate drive circuits, modulator configurations and circuit topologies. Power metal oxide semiconductor field effect transistors (MOSFETS) were chosen as the switch element because of their high repetition rate capability, fast turn-on and turn-off times, low control power and high reliability.

The circuit topology required to achieve the high repetition rate, variable pulse width, and reset of the induction core is quite complex. Computer modeling is necessary for analyzing circuit behavior, flux trajectories, and stray elements. A PSpice model has been developed to simulate the modulator's circuit performance and induction core flux behavior [4]. In this paper we will show the development and validation of the models for key network elements, the results of PSpice simulations of a complex switch array with four parallel stacks of six switches in series, and comparisons with measured data.

The Circuit

The simplified circuit shown in Figure 1 represents the modulator prototype. The modulator consists of an energy storage bank, a switching element, an induction cell and a cell reset circuit. Modulator operation can be explained the following way: The energy storage bank is precharged to the desired accelerating potential. On command, the series-parallel array of MOSFET switches close and the storage capacitor is connected to the induction cell. The load is primarily the magnetization current required of the Metglas [5] in the induction cell. The cell voltage provides the potential to accelerate the ion beam through the induction cell. When the MOSFET switches open ending the accelerating pulse, the cell current is diverted to the reset capacitor through a fast diode array. The reset circuit drives the cell to the original magnetic

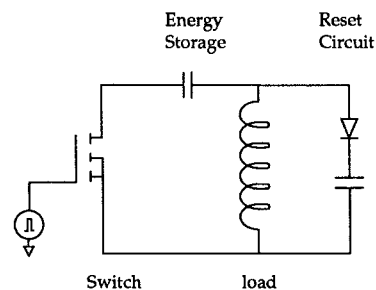


Figure 1. Simplified circuit diagram of the recirculator modulator.

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state between pulses by diverting the stored energy in the core to the reset capacitor. The voltage on the reset capacitor is regulated to stabilize the reset voltage and determine the rate of cell reset.

Modeling

Computer modeling is necessary for the network design and optimization. The modeling objectives were to accurately predict circuit behavior, to understand MOSFET switch operating conditions, and to develop confidence in applying the code to future generation machines. The core model in PSpice uses the Jiles-Atherton model for analyzing non-linear cores [6]. This model was adjusted to simulate the Metglas core.

Several parameters are used to describe the shape of the magnetic hysteresis in the PSpice model. These parameters include the saturation magnetization, M_S , and the thermal energy parameter, A . Characterizing the core material was done by a trial and error using PSpice. The traditional loop was generated by ramping the current through a test core model and displaying the B-H loop. First, the anhystretic curve was determined by setting the saturation flux density, $M_S = B_{max}/0.01257$. All units in the model are MKS. Once this is set, the slope of the anhystretic loop or material permeability is set by setting the inter domain coupling parameter using the relationship slope = $1/(3 \cdot A/M_S)$. Next, the core losses are added to the model by varying the "drag", K . This parameter was determined by plotting where the hysteresis loop crossed the H axis as a function of "K" in the core model and observing the trends. In addition, PSpice has added a rate change function to their model, γ , which varies the widening of the loop with respect to frequency. This parameter was adjusted and models were run with three different current ramp rates and the results were observed and changes were made to "K" and γ as needed to match core data. Verification of the model was made by calculating the core losses from the hysteresis and comparing the results with small core test data and an empirical core loss equation from Kuenning [7]: Figure 2.

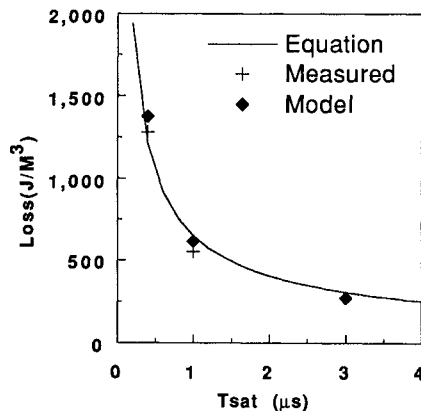


Figure 2. Plot of small core loss data showing good agreement between measured data, an empirical equation, and PSpice simulation for 2605S-3A Metglas.

A simple switch model was incorporated for the MOSFET switch array. The model utilizes the PSpice voltage dependent switch. A capacitor was placed in parallel with the switch to represent the drain-source capacitance of the MOSFET switch array. A series inductance was also added to model the switch inductance. In an attempt to model the turn-on characteristics of the MOSFET switch, the controlling voltage of the switch was driven through a RC network to slow the gate voltage rise time. These network elements were used to model a modulator with four parallel strings of six MOSFETS in series (6X4). The network diagram for the 6X4 modulator, Figure 3, shows the four energy storage capacitor banks, four switching branches, and four reset circuits connected in four quadrants driving the Metglas core.

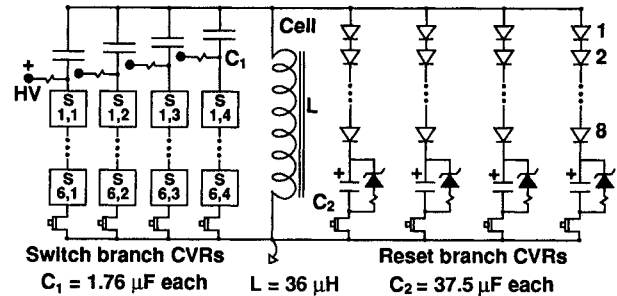


Figure 3. Circuit architecture of the 6X4 modulator.

Simulation results

The PSpice network model is shown in Figure 4. This model represents the 6X4 modulator with the four switch, snubber, and reset circuits combined into one lumped network to represent the modulator configuration. The series switch stack and snubbers were modeled as a single switch element. The main capacitor banks were also combined into a single element. The stray elements used in the model were a lumped simplification and do not represent their physical origins.

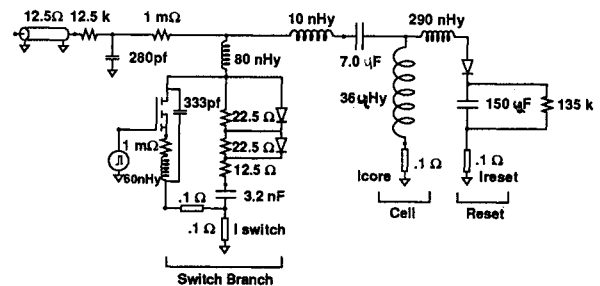


Figure 4. The PSpice network model of the 6X4 modulator.

The simulation shows the main voltage and current features in addition to the reset and flux behavior. The circuit simulations were compared with measured machine data. Figures 5a and 5b show comparisons between the simulated and measured data for the switch and reset branch currents. The switch branch currents and the reset branch currents were measured with current viewing resistors, digitized, then added together and overlaid with the simulation results. Figure 6 shows an overlay of the simulated and measured core voltage. As shown in Figures 5 and 6, reasonably good agreement was obtained between the model and data.

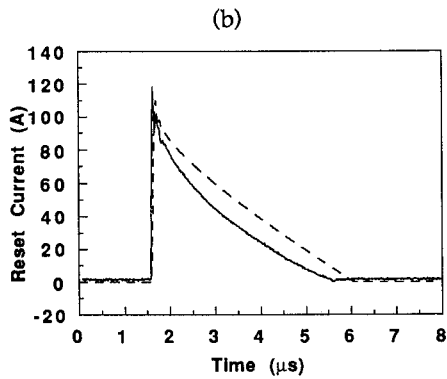
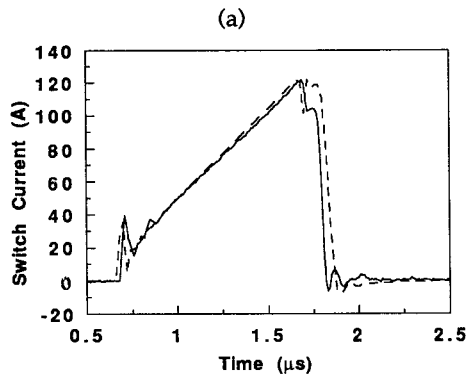


Figure 5. Single pulse comparisons between measured data (solid line) and model simulations (dashed line): (a) Total switch current. (b) Total reset current

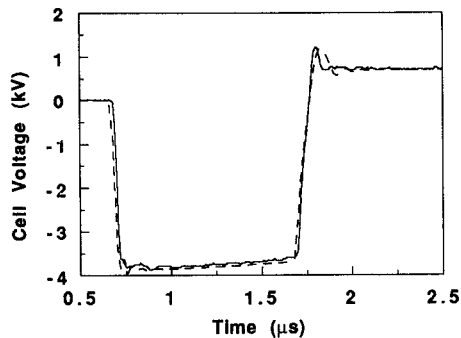


Figure 6. Core voltage comparison between measured (solid line) and modeled data (dashed line).

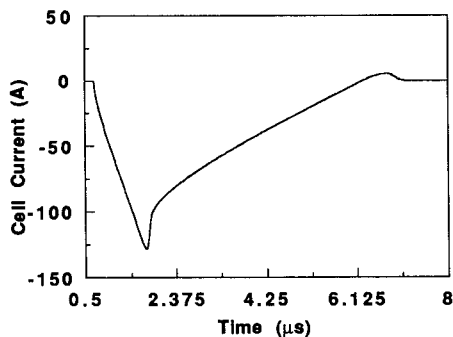


Figure 7. PSpice simulation of whole core current

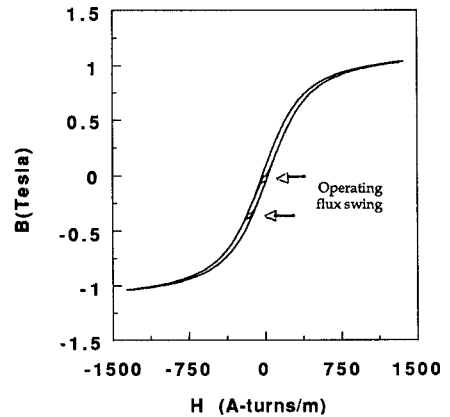


Figure 8. Overlay of the saturated model with the normal machine hysteresis loop.

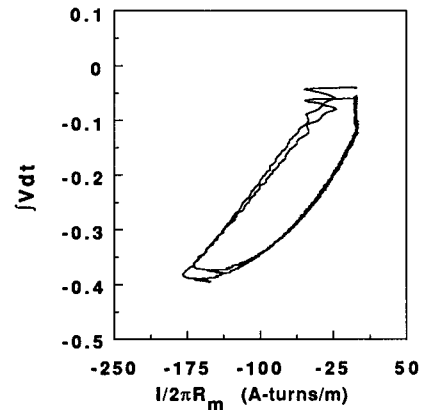


Figure 9. Two terminal measurement of the machine B-H loop trajectory during multipulse operation.

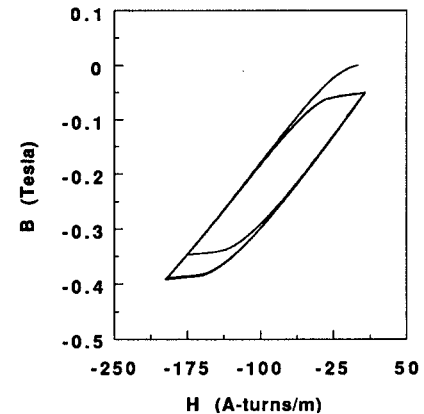


Figure 10. PSpice simulation of the cores B-H loop for a 4 pulse burst.

The model enables us to observe circuit performance in areas where diagnostic measurements are not practical. For example, Figure 7 represents the modeled whole core current. In another example, a linear current source was used to drive the magnetic core model to saturation for two cycles and is shown in Figure 8. The machines operating hysteresis loop has been overlaid with the saturated model to show that during normal machine operation, the working flux swing is only a

small fraction of the total flux swing available. Because of this small flux swing, core losses have been reduced during machine operation.

It is a concern that the system achieve complete reset of the core because insufficient reset would eventually saturate the core after a number pulses. The nonlinear core model was needed to analyze the behavior of the reset circuit. Figure 9 illustrates the magnetic hysteresis for three cycles. The magnetic path is observed to walk during the first cycle and then it reaches stabilization. A comparison of the model hysteresis with that of the machine is shown in Figures 9 and 10. Although there are differences in their behavior, the magnetic model proved to be a key element in the system model. Figure 11 illustrates the differences in circuit behavior with and without the core model. The core model provided the circuit information necessary to closely match the machine output wave forms.

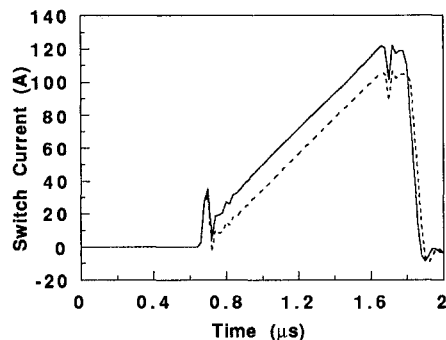


Figure 11. Comparison of the PSpice simulation of total switch current with (solid line) and without (dashed line) the non-linear core model

Summary

We have developed a modeling tool for designing and analyzing high repetition rate MOSFET modulators for

induction accelerators. The circuit model agrees well with measured data and is being used for the design of the next generation modulator. These simulations address only the power flow of the modulator. More comprehensive modeling of the MOSFET switch array, switch protection elements, and modulator recharge network is needed. We are now working to develop a dynamic core model that incorporates rate change effects and should predict core losses with greater accuracy. In addition, we are developing new switch models based on the PSpice MOSFET switch model with the parameters adjusted to reflect the behavior of the system array.

References

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